华澜微电子
HUALAN
MICROELECTRONIQUE

36-Port 12Gbps SAS Expander

HL7721

Datasheet

Version 1.16

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Revision History

Revision	Date	Description
V0.01	2022/8/25	Draft version.
V1.00	2023/10/19	Added typical application scenarios.
V1.08	2024/3/11	1. Refine the Power on and reset timing; 2. Modify VDDIO18 description. Separate GPIO DC character to 1.8V part and 3.3V part; 3. Remove PHY0_CKREFPO & PHY0_CKREFNO because they are useless for users; 4. Remove eJTAG since it's not supported currently.
V1.13	2024/8/16	1. Added thermal data; 2. Updated VDDIO1，VDDIO2 and VDDIO3 power supply requirement.
V1.14	2024/11/22	1. Modify electrical characteristic per actual test result.
V1.15	2024/12/11	1. Modify storage temperature to -40℃~125℃; 2. Added Junction operating temperature.
V1.16	2025/6/9	1. Modify VDDA_PLL Power supply as: default is disconnection.

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CHAPTER 1 GENERAL DESCRIPTION

HL7721 is 36-port SAS 12G expander controller for storage servers and computing servers. HL7721 support both fanout expander and edge expander application.

It features speed equalization(SEM), SAS-3 T10 zoning, self-configuration, SMART management and SES support for enclosure management. It is compatible with SAS 12G/6G/3G and SATA 6G/3G/1.5G. It supports HDD/SSD directly attach and expander cascade routing.

HL7721 integrate a high-performance RISC-V microprocessor, a secure encryption authentication engine and other peripherals control logic. 118 GPIO pins can be flexibly configured as various standard interface application.

HL7721 is space optimized for server backplane and other implementations requiring a small footprint solution for storage expansion. It is designed for expanding large quantity of drives in which storage controllers requiring SAS/SATA interface. It provides a high-performance, high-capacity SAS/SATA device to be used in high availability (HA) enterprise storage systems, with performance aggregation and security solutions.

1.1. HL7721 SAS Expander Architecture

The HL7721 SAS expander's architecture is shown as figure 1.1. There are 36 physical SAS ports and 3 virtual SAS ports, one High-Performance RISC-V Cores with 1M byte ITCM and 2M byte DTCM. Peripheral interfaces offers various protocols such as UART, I2C, SGPIO, QSPI and eMMC.

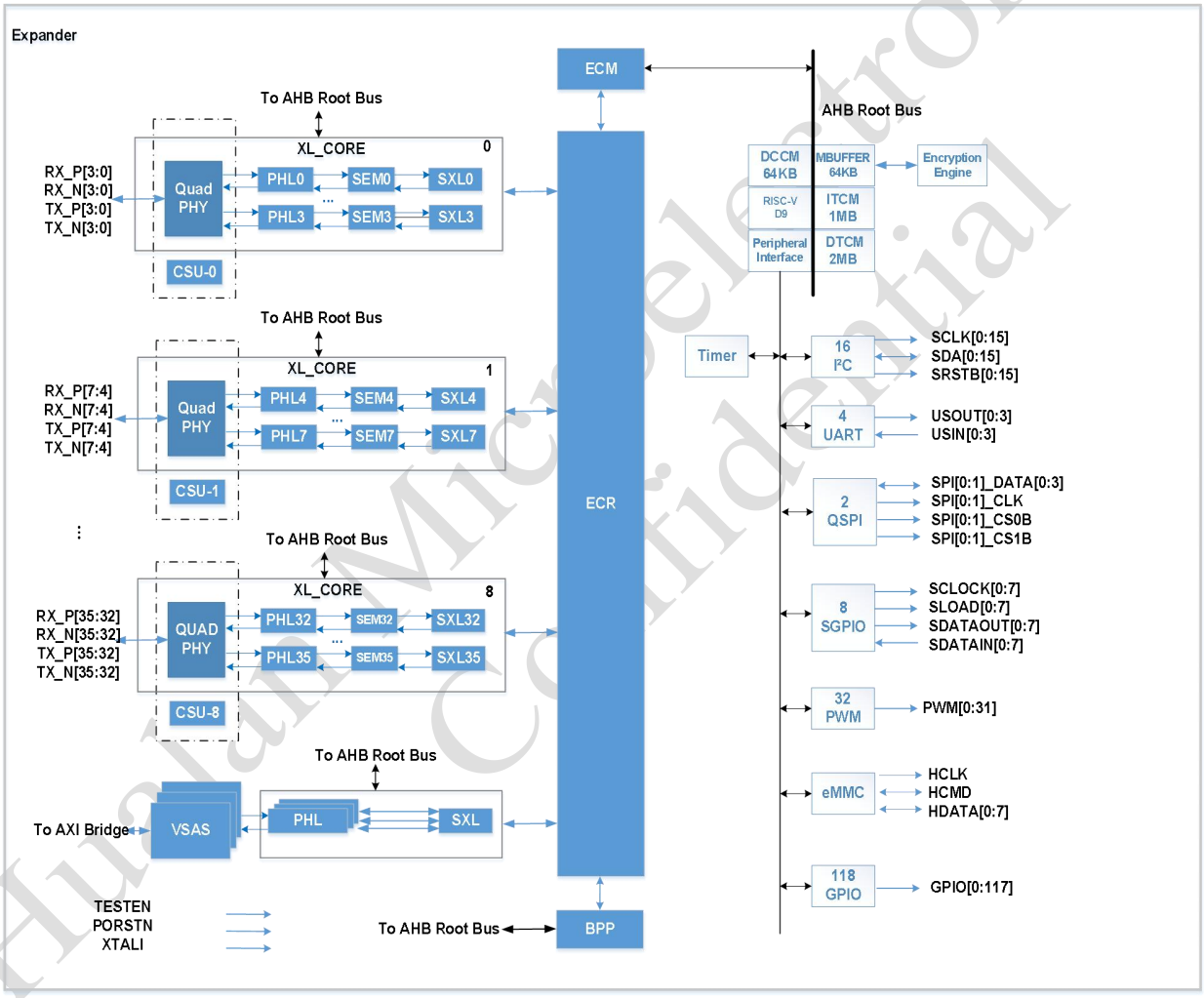


Figure 1.1 HL7721 36-Port 12Gbps SAS Expander Architecture

1.2. Typical Application

The HL7721 expander is fully compatible with the main stream RAID adapters and HBAs, allowing seamless integration and management with end-to-end solution. It has been tested for interoperability with a wide variety of SAS and SATA HDDs/ SSDs.

The HL7721 enables efficient designs supporting up to 28 drive bays and two ×4 wideports uplink for ingress and expansion.

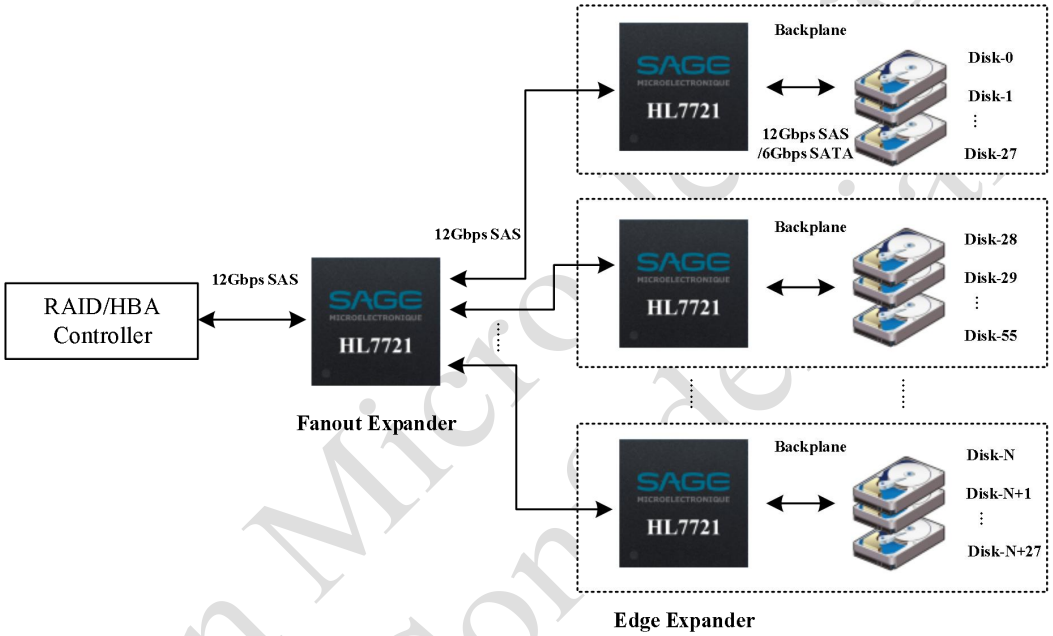


Figure 1.2 HL7721 Application I: Cascaded Two-level Storage Expansion

HL7721 is ideal for massive storage expansion that require low-cost and low power solution, that is, the eight HL7721 can be cascaded connected for up to eight level and they can support more than 200 disks.

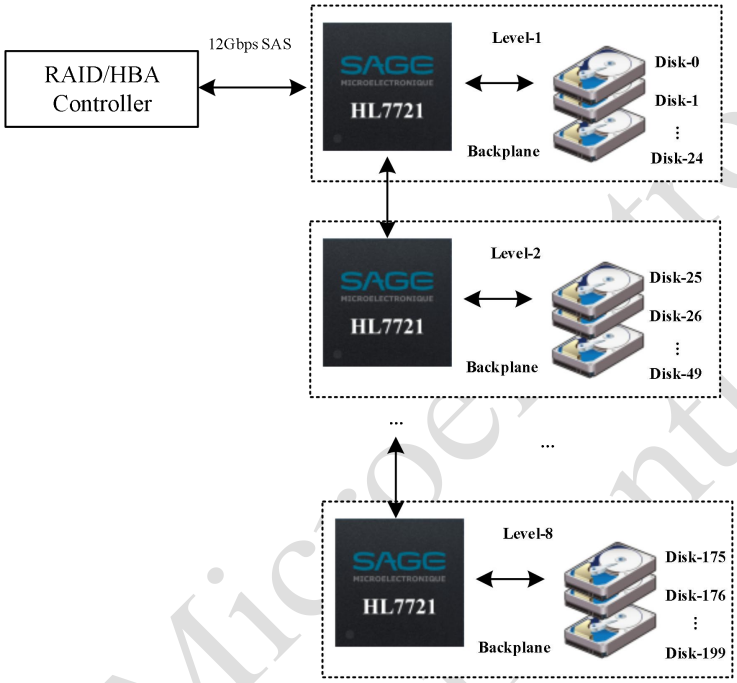


Figure 1.3 HL7721 Application II: Cascaded Eight-level Storage Expansion

CHAPTER 2 FEATURE

2.1. General

- SAS-3 T10 zoning for secure storage (up to 256 zone format).
- Ultra low switching latency for improved system performance.
- Edge-buffering speed equalization module (SEM) .
- Multi-initiator up to 16 initiators.
- Adaptive matching between SAS and SATA interface.
- Direct, Table and Substractive routing methods.
- 4096 route table entries.
- SES support for enclosure management.
- 12G SAS signaling support for mini-SAS HD passive copper cable.
- SAS Optical mode support.
- Disk Spin-Up.
- Quad SPI flash support.
- Early power off warning (EPOW).
- Low PHY power conditions support.
- Inter-Expander communication.
- Port mirroring for system debug.
- Mass log storage for debug use.
- Real-time eye capture with enhanced BER eye mask and estimation.
- Non-disruptive zero down time firmware update support.
- Position-independent firmware image support to simplify firmware image management/download.
- <12W power consumption in full-load operation state.

2.2. High Speed I/O

- SAS (12 Gbps, 6 Gbps, 3 Gbps, 1.5 Gbps) and SATA (6 Gbps, 3 Gbps, 1.5 Gbps) operation.
- Link adaptation

  -Adaptive or programmable 3-tap TX feed forward equalizer(FFE).

-Adaptive or programmable RX continuous time linear equalization (CTLE) and 5-tap decision feedback equalization (DFE).

- Support spread-spectrum clocking (SSC) .
- Per-PHY programmable transmit amplitude and emphasis.
- Automatic speed negotiation.

2.3. Security

- HW support safety FW boot load.
- Embedded Encryption/Decryption hardware module.
- Security Algorithms: AES128/256, SM4, SM3, SM2,SHA, RSA3072/4096.
- On-chip true random number generator.

2.4. Peripheral Interface

- Configurable 118 GPIO pins for standard peripheral interfaces.
- 16 I^2C interfaces to support hot-plug in master or slave mode[1].
- 8 SGPIO interfaces.
- 4 UART interfaces for system monitoring and debugging.
- 2 SPI/QSPI interfaces.
- External NOR flash for FW storage.
- 1 eMMC interface for mass application storage.
- PWM based LED for link status and fault indication.

Note[1]: I^2C-0 can be configured as master or slave. I^2C-1~I^2C-15 can only be configured as I^2C master.

2.5. Configuration and Management Tool

- PHY configuration and management.
- Firmware download over multiple in-band and out-of-band interfaces.
- SAM4/SPC4/SES3-compatible SES target with Enclosure Management Application reference design.

- PHY Topology Viewer.
- Per-port error counters.
- Error detection, logging, and reporting.
- Digital eye diagram support.
- SMART feature support.
- Zoning configuration interface.

2.6. Package

- FCBGA 1059 27x27mm.

CHAPTER 3 PIN DESCRIPTION

3.1. Ball map

Figure 3.1 illustrates the 1059-Ball FCBGA 27 × 27 mm ball diagram for the HL7721.

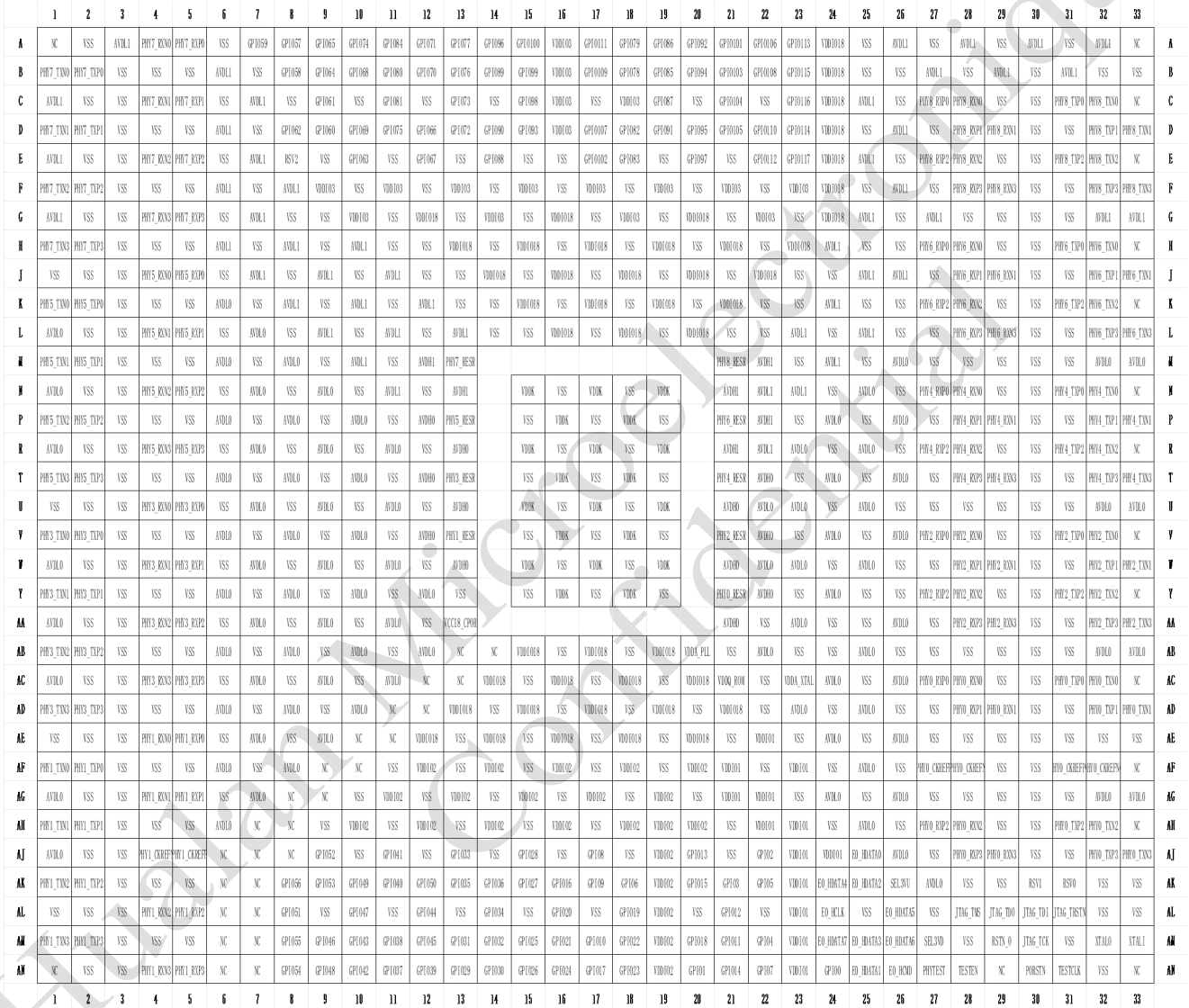


Figure 3.1 HL7721 FCBGA Ball Map

3.2. Signal Description

The signal types and definitions is shown as below,

Signal Type	Definition
A	Analog
D	Digital
I/O	Input and Output
I	Input Only
O	Output Only
OC	Open Collector
OD	Open-Drain Pad
Ground	Ground
P	Power
NC	No Connect
DNC	Do Not Connect

3.2.1. System Signals

Table 3.1 System Signals

Signal Name	Description	Signal Number	Type
TESTEN	Test mode enable select, active high (0=normal mode, 1= test mode). Default must connect to GND with resistor.	AN28	DI
PORSTN	Reset signal input, active low	AN30	DI
RSTN_O	Internal POR（Power on reset）signal output，active low, can wire AND with PORSTN (connect 0 ohms resistor to PORSTN).	AM29	DO
SEL3VU	1.8/3.3V VDDIO selection for GPIO57~117 (0=1.8V, 1=3.3V).	AK26	DI
SEL3VD	1.8/3.3V VDDIO selection for GPIO0~56(0=1.8V, 1=3.3V).	AM27	DI

3.2.2. SAS/SATA Interface

Table 3.2 SAS/SATA Interface Signals

Signal Name	Description	Signal Number	Type
PHY0_RXP0	PHY0 differential data input of RX for lane 0, positive, data rate up to 12Gbps	AC27	AI
PHY0_RXN0	PHY0 differential data input of RX for lane 0, negative, data rate up to 12Gbps	AC28	AI
PHY0_TXP0	PHY0 differential data output of TX for lane 0, positive, data rate up to 12Gbps	AC31	AO
PHY0_TXN0	PHY0 differential data output of TX for lane 0, negative, data rate up to 12Gbps	AC32	AO
PHY0_RXP1	PHY0 differential data input of RX for lane 1, positive, data rate up to 12Gbps	AD28	AI
PHY0_RXN1	PHY0 differential data input of RX for lane 1, negative, data rate up to 12Gbps	AD29	AI
PHY0_TXP1	PHY0 differential data output of TX for lane 1, positive, data rate up to 12Gbps	AD32	AO
PHY0_TXN1	PHY0 differential data output of TX for lane 1, negative, data rate up to 12Gbps	AD33	AO
PHY0_CKREFP	PHY0 Differential reference clock input, positive. Effective for PHY0~PHY8	AF27	DI
PHY0_CKREFN	PHY0 Differential reference clock input, negative. Effective for PHY0~PHY8	AF28	DI
PHY0_RESR	PHY0 reference resistor for termination calibration, Connect 200ohms to GND	Y21	AO
PHY0_TXN2	PHY0 differential data output of TX for lane 2, negative, data rate up to 12Gbps	AH32	AO
PHY0_TXP2	PHY0 differential data output of TX for lane 2, positive, data rate up to 12Gbps	AH31	AO
PHY0_RXN2	PHY0 differential data input of RX for lane 2, negative, data rate up to 12Gbps	AH28	AI
PHY0_RXP2	PHY0 differential data input of RX for lane 2, positive, data rate up to 12Gbps	AH27	AI
PHY0_TXN3	PHY0 differential data output of TX for lane 3, negative, data rate up to 12Gbps	AJ33	AO
PHY0_TXP3	PHY0 differential data output of TX for lane 3, positive, data	AJ32	AO

	rate up to 12Gbps		
PHY0_RXN3	PHY0 differential data input of RX for lane 3, negative, data rate up to 12Gbps	AJ29	AI
PHY0_RXP3	PHY0 differential data input of RX for lane 3, positive, data rate up to 12Gbps	AJ28	AI
PHY1_RXP0	PHY1 differential data input of RX for lane 0, positive, data rate up to 12Gbps	AE5	AI
PHY1_RXN0	PHY1 differential data input of RX for lane 0, negative, data rate up to 12Gbps	AE4	AI
PHY1_TXP0	PHY1 differential data output of TX for lane 0, positive, data rate up to 12Gbps	AF2	AO
PHY1_TXN0	PHY1 differential data output of TX for lane 0, negative, data rate up to 12Gbps	AF1	AO
PHY1_RXP1	PHY1 differential data input of RX for lane 1, positive, data rate up to 12Gbps	AG5	AI
PHY1_RXN1	PHY1 differential data input of RX for lane 1, negative, data rate up to 12Gbps	AG4	AI
PHY1_TXP1	PHY1 differential data output of TX for lane 1, positive, data rate up to 12Gbps	AH2	AO
PHY1_TXN1	PHY1 differential data output of TX for lane 1, negative, data rate up to 12Gbps	AH1	AO
PHY1_RESR	PHY1 reference resistor for termination calibration, Connect 200ohms to GND	V13	AO
PHY1_TXN2	PHY1 differential data output of TX for lane 2, negative, data rate up to 12Gbps	AK1	AO
PHY1_TXP2	PHY1 differential data output of TX for lane 2, positive, data rate up to 12Gbps	AK2	AO
PHY1_RXN2	PHY1 differential data input of RX for lane 2, negative, data rate up to 12Gbps	AL4	AI
PHY1_RXP2	PHY1 differential data input of RX for lane 2, positive, data rate up to 12Gbps	AL5	AI
PHY1_TXN3	PHY1 differential data output of TX for lane 3, negative, data rate up to 12Gbps	AM1	AO
PHY1_TXP3	PHY1 differential data output of TX for lane 3, positive, data rate up to 12Gbps	AM2	AO
PHY1_RXN3	PHY1 differential data input of RX for lane 3, negative, data rate up to 12Gbps	AN4	AI

PHY1_RXP3	PHY1 differential data input of RX for lane 3, positive, data rate up to 12Gbps	AN5	AI
PHY2_RXP0	PHY2 differential data input of RX for lane 0, positive, data rate up to 12Gbps	V27	AI
PHY2_RXN0	PHY2 differential data input of RX for lane 0, negative, data rate up to 12Gbps	V28	AI
PHY2_TXP0	PHY2 differential data output of TX for lane 0, positive, data rate up to 12Gbps	V31	AO
PHY2_TXN0	PHY2 differential data output of TX for lane 0, negative, data rate up to 12Gbps	V32	AO
PHY2_RXP1	PHY2 differential data input of RX for lane 1, positive, data rate up to 12Gbps	W28	AI
PHY2_RXN1	PHY2 differential data input of RX for lane 1, negative, data rate up to 12Gbps	W29	AI
PHY2_TXP1	PHY2 differential data output of TX for lane 1, positive, data rate up to 12Gbps	W32	AO
PHY2_TXN1	PHY2 differential data output of TX for lane 1, negative, data rate up to 12Gbps	W33	AO
PHY2_RESR	PHY2 reference resistor for termination calibration, Connect 200ohms to GND	V21	AO
PHY2_TXN2	PHY2 differential data output of TX for lane 2, negative, data rate up to 12Gbps	Y32	AO
PHY2_TXP2	PHY2 differential data output of TX for lane 2, positive, data rate up to 12Gbps	Y31	AO
PHY2_RXN2	PHY2 differential data input of RX for lane 2, negative, data rate up to 12Gbps	Y28	AI
PHY2_RXP2	PHY2 differential data input of RX for lane 2, positive, data rate up to 12Gbps	Y27	AI
PHY2_TXN3	PHY2 differential data output of TX for lane 3, negative, data rate up to 12Gbps	AA33	AO
PHY2_TXP3	PHY2 differential data output of TX for lane 3, positive, data rate up to 12Gbps	AA32	AO
PHY2_RXN3	PHY2 differential data input of RX for lane 3, negative, data rate up to 12Gbps	AA29	AI
PHY2_RXP3	PHY2 differential data input of RX for lane 3, positive, data rate up to 12Gbps	AA28	AI
PHY3_RXP0	PHY3 differential data input of RX for lane 0, positive, data	U5	AI

	rate up to 12Gbps		
PHY3_RXN0	PHY3 differential data input of RX for lane 0, negative, data rate up to 12Gbps	U4	AI
PHY3_TXP0	PHY3 differential data output of TX for lane 0, positive, data rate up to 12Gbps	V2	AO
PHY3_TXN0	PHY3 differential data output of TX for lane 0, negative, data rate up to 12Gbps	V1	AO
PHY3_RXP1	PHY3 differential data input of RX for lane 1, positive, data rate up to 12Gbps	W5	AI
PHY3_RXN1	PHY3 differential data input of RX for lane 1, negative, data rate up to 12Gbps	W4	AI
PHY3_TXP1	PHY3 differential data output of TX for lane 1, positive, data rate up to 12Gbps	Y2	AO
PHY3_TXN1	PHY3 differential data output of TX for lane 1, negative, data rate up to 12Gbps	Y1	AO
PHY3_RESR	PHY3 reference resistor for termination calibration, Connect 200ohms to GND	T13	AO
PHY3_TXN2	PHY3 differential data output of TX for lane 2, negative, data rate up to 12Gbps	AB1	AO
PHY3_TXP2	PHY3 differential data output of TX for lane 2, positive, data rate up to 12Gbps	AB2	AO
PHY3_RXN2	PHY3 differential data input of RX for lane 2, negative, data rate up to 12Gbps	AA4	AI
PHY3_RXP2	PHY3 differential data input of RX for lane 2, positive, data rate up to 12Gbps	AA5	AI
PHY3_TXN3	PHY3 differential data output of TX for lane 3, negative, data rate up to 12Gbps	AD1	AO
PHY3_TXP3	PHY3 differential data output of TX for lane 3, positive, data rate up to 12Gbps	AD2	AO
PHY3_RXN3	PHY3 differential data input of RX for lane 3, negative, data rate up to 12Gbps	AC4	AI
PHY3_RXP3	PHY3 differential data input of RX for lane 3, positive, data rate up to 12Gbps	AC5	AI
PHY4_RXP0	PHY4 differential data input of RX for lane 0, positive, data rate up to 12Gbps	N27	AI
PHY4_RXN0	PHY4 differential data input of RX for lane 0, negative, data rate up to 12Gbps	N28	AI

PHY4_TXP0	PHY4 differential data output of TX for lane 0, positive, data rate up to 12Gbps	N31	AO
PHY4_TXN0	PHY4 differential data output of TX for lane 0, negative, data rate up to 12Gbps	N32	AO
PHY4_RXP1	PHY4 differential data input of RX for lane 1, positive, data rate up to 12Gbps	P28	AI
PHY4_RXN1	PHY4 differential data input of RX for lane 1, negative, data rate up to 12Gbps	P29	AI
PHY4_TXP1	PHY4 differential data output of TX for lane 1, positive, data rate up to 12Gbps	P32	AO
PHY4_TXN1	PHY4 differential data output of TX for lane 1, negative, data rate up to 12Gbps	P33	AO
PHY4_RESR	PHY4 reference resistor for termination calibration, Connect 200ohms to GND	T21	AO
PHY4_TXN2	PHY4 differential data output of TX for lane 2, negative, data rate up to 12Gbps	R32	AO
PHY4_TXP2	PHY4 differential data output of TX for lane 2, positive, data rate up to 12Gbps	R31	AO
PHY4_RXN2	PHY4 differential data input of RX for lane 2, negative, data rate up to 12Gbps	R28	AI
PHY4_RXP2	PHY4 differential data input of RX for lane 2, positive, data rate up to 12Gbps	R27	AI
PHY4_TXN3	PHY4 differential data output of TX for lane 3, negative, data rate up to 12Gbps	T33	AO
PHY4_TXP3	PHY4 differential data output of TX for lane 3, positive, data rate up to 12Gbps	T32	AO
PHY4_RXN3	PHY4 differential data input of RX for lane 3, negative, data rate up to 12Gbps	T29	AI
PHY4_RXP3	PHY4 differential data input of RX for lane 3, positive, data rate up to 12Gbps	T28	AI
PHY5_RXP0	PHY5 differential data input of RX for lane 0, positive, data rate up to 12Gbps	J5	AI
PHY5_RXN0	PHY5 differential data input of RX for lane 0, negative, data rate up to 12Gbps	J4	AI
PHY5_TXP0	PHY5 differential data output of TX for lane 0, positive, data rate up to 12Gbps	K2	AO
PHY5_TXN0	PHY5 differential data output of TX for lane 0, negative, data	K1	AO

	rate up to 12Gbps		
PHY5_RXP1	PHY5 differential data input of RX for lane 1, positive, data rate up to 12Gbps	L5	AI
PHY5_RXN1	PHY5 differential data input of RX for lane 1, negative, data rate up to 12Gbps	L4	AI
PHY5_TXP1	PHY5 differential data output of TX for lane 1, positive, data rate up to 12Gbps	M2	AO
PHY5_TXN1	PHY5 differential data output of TX for lane 1, negative, data rate up to 12Gbps	M1	AO
PHY5_RESR	PHY5 reference resistor for termination calibration, Connect 200ohms to GND	P13	AO
PHY5_TXN2	PHY5 differential data output of TX for lane 2, negative, data rate up to 12Gbps	P1	AO
PHY5_TXP2	PHY5 differential data output of TX for lane 2, positive, data rate up to 12Gbps	P2	AO
PHY5_RXN2	PHY5 differential data input of RX for lane 2, negative, data rate up to 12Gbps	N4	AI
PHY5_RXP2	PHY5 differential data input of RX for lane 2, positive, data rate up to 12Gbps	N5	AI
PHY5_TXN3	PHY5 differential data output of TX for lane 3, negative, data rate up to 12Gbps	T1	AO
PHY5_TXP3	PHY5 differential data output of TX for lane 3, positive, data rate up to 12Gbps	T2	AO
PHY5_RXN3	PHY5 differential data input of RX for lane 3, negative, data rate up to 12Gbps	R4	AI
PHY5_RXP3	PHY5 differential data input of RX for lane 3, positive, data rate up to 12Gbps	R5	AI
PHY6_RXP0	PHY6 differential data input of RX for lane 0, positive, data rate up to 12Gbps	H27	AI
PHY6_RXN0	PHY6 differential data input of RX for lane 0, negative, data rate up to 12Gbps	H28	AI
PHY6_TXP0	PHY6 differential data output of TX for lane 0, positive, data rate up to 12Gbps	H31	AO
PHY6_TXN0	PHY6 differential data output of TX for lane 0, negative, data rate up to 12Gbps	H32	AO
PHY6_RXP1	PHY6 differential data input of RX for lane 1, positive, data rate up to 12Gbps	J28	AI

PHY6_RXN1	PHY6 differential data input of RX for lane 1, negative, data rate up to 12Gbps	J29	AI
PHY6_TXP1	PHY6 differential data output of TX for lane 1, positive, data rate up to 12Gbps	J32	AO
PHY6_TXN1	PHY6 differential data output of TX for lane 1, negative, data rate up to 12Gbps	J33	AO
PHY6_RESR	PHY6 reference resistor for termination calibration, Connect 200ohms to GND	P21	AO
PHY6_TXN2	PHY6 differential data output of TX for lane 2, negative, data rate up to 12Gbps	K32	AO
PHY6_TXP2	PHY6 differential data output of TX for lane 2, positive, data rate up to 12Gbps	K31	AO
PHY6_RXN2	PHY6 differential data input of RX for lane 2, negative, data rate up to 12Gbps	K28	AI
PHY6_RXP2	PHY6 differential data input of RX for lane 2, positive, data rate up to 12Gbps	K27	AI
PHY6_TXN3	PHY6 differential data output of TX for lane 3, negative, data rate up to 12Gbps	L33	AO
PHY6_TXP3	PHY6 differential data output of TX for lane 3, positive, data rate up to 12Gbps	L32	AO
PHY6_RXN3	PHY6 differential data input of RX for lane 3, negative, data rate up to 12Gbps	L29	AI
PHY6_RXP3	PHY6 differential data input of RX for lane 3, positive, data rate up to 12Gbps	L28	AI
PHY7_RXP0	PHY7 differential data input of RX for lane 0, positive, data rate up to 12Gbps	A5	AI
PHY7_RXN0	PHY7 differential data input of RX for lane 0, negative, data rate up to 12Gbps	A4	AI
PHY7_TXP0	PHY7 differential data output of TX for lane 0, positive, data rate up to 12Gbps	B2	AO
PHY7_TXN0	PHY7 differential data output of TX for lane 0, negative, data rate up to 12Gbps	B1	AO
PHY7_RXP1	PHY7 differential data input of RX for lane 1, positive, data rate up to 12Gbps	C5	AI
PHY7_RXN1	PHY7 differential data input of RX for lane 1, negative, data rate up to 12Gbps	C4	AI
PHY7_TXP1	PHY7 differential data output of TX for lane 1, positive, data	D2	AO

	rate up to 12Gbps		
PHY7_TXN1	PHY7 differential data output of TX for lane 1, negative, data rate up to 12Gbps	D1	AO
PHY7_RESR	PHY7 reference resistor for termination calibration, Connect 200ohms to GND	M13	AO
PHY7_TXN2	PHY7 differential data output of TX for lane 2, negative, data rate up to 12Gbps	F1	AO
PHY7_TXP2	PHY7 differential data output of TX for lane 2, positive, data rate up to 12Gbps	F2	AO
PHY7_RXN2	PHY7 differential data input of RX for lane 2, negative, data rate up to 12Gbps	E4	AI
PHY7_RXP2	PHY7 differential data input of RX for lane 2, positive, data rate up to 12Gbps	E5	AI
PHY7_TXN3	PHY7 differential data output of TX for lane 3, negative, data rate up to 12Gbps	H1	AO
PHY7_TXP3	PHY7 differential data output of TX for lane 3, positive, data rate up to 12Gbps	H2	AO
PHY7_RXN3	PHY7 differential data input of RX for lane 3, negative, data rate up to 12Gbps	G4	AI
PHY7_RXP3	PHY7 differential data input of RX for lane 3, positive, data rate up to 12Gbps	G5	AI
PHY8_RXP0	PHY8 differential data input of RX for lane 0, positive, data rate up to 12Gbps	C27	AI
PHY8_RXN0	PHY8 differential data input of RX for lane 0, negative, data rate up to 12Gbps	C28	AI
PHY8_TXP0	PHY8 differential data output of TX for lane 0, positive, data rate up to 12Gbps	C31	AO
PHY8_TXN0	PHY8 differential data output of TX for lane 0, negative, data rate up to 12Gbps	C32	AO
PHY8_RXP1	PHY8 differential data input of RX for lane 1, positive, data rate up to 12Gbps	D28	AI
PHY8_RXN1	PHY8 differential data input of RX for lane 1, negative, data rate up to 12Gbps	D29	AI
PHY8_TXP1	PHY8 differential data output of TX for lane 1, positive, data rate up to 12Gbps	D32	AO
PHY8_TXN1	PHY8 differential data output of TX for lane 1, negative, data rate up to 12Gbps	D33	AO

PHY8_RESR	PHY8 reference resistor for termination calibration, Connect 200ohms to GND	M21	AO
PHY8_TXN2	PHY8 differential data output of TX for lane 2, negative, data rate up to 12Gbps	E32	AO
PHY8_TXP2	PHY8 differential data output of TX for lane 2, positive, data rate up to 12Gbps	E31	AO
PHY8_RXN2	PHY8 differential data input of RX for lane 2, negative, data rate up to 12Gbps	E28	AI
PHY8_RXP2	PHY8 differential data input of RX for lane 2, positive, data rate up to 12Gbps	E27	AI
PHY8_TXN3	PHY8 differential data output of TX for lane 3, negative, data rate up to 12Gbps	F33	AO
PHY8_TXP3	PHY8 differential data output of TX for lane 3, positive, data rate up to 12Gbps	F32	AO
PHY8_RXN3	PHY8 differential data input of RX for lane 3, negative, data rate up to 12Gbps	F29	AI
PHY8_RXP3	PHY8 differential data input of RX for lane 3, positive, data rate up to 12Gbps	F28	AI
PHYTEST	PHY digital output. Only for internal debug purpose	AN27	DO

3.2.3. Clock Interface

Table 3.3 Clock Interface Signals

Signal Name	Description	Signal Number	Type
XTALI	**Crystal Input/Oscillator Input.** It is connected to a 25MHz crystal or oscillator.	AM33	AI
XTALO	**Crystal Output.** It is connected to a crystal. While oscillator is applied, this pin should be reserved for No Connection (NC).	AM32	AO
TESTCLK	Optional reference clock 25MHz input for ATPG test.	AN31	AI

3.2.4. Peripheral Interface

The flexible I/O structure allows users to program the I/O features by firmware.

Users can program the pull-up, pull-down for the input functions. Section 4.3 shows the input pull-up resistance and input pull-down resistance.

Each GPIO can configurable to four function by firmware. The function 0 is GPIO mode while other function can be configured as I²C/SGPIO/SFLASH/UART.

The detail configuration is shown on the table as below,

Table 3.4 Programmable GPIO Configuration

Signal Name (Function 0)	Function1 (Default)	Function 2	Function 3	Signal Number	Boot Strap
GPIO0	SCLK[0] I²C-0	/	/	AN24	DIO
GPIO1	SDA[0] I²C-0	/	/	AN20	DIO
GPIO2	SRSTB[0] I²C-0	PWM0	/	AJ22	DIO
GPIO3	SCLK[1] I²C-1	/	/	AK21	DIO
GPIO4	SDA[1] I²C-1	/	/	AM22	DIO
GPIO5	SRSTB[1] I²C-1	PWM1	/	AK22	DIO
GPIO6	SCLK[2] I²C-2	/	/	AK18	DIO
GPIO7	SDA[2] I²C-2	/	/	AN22	DIO
GPIO8	SRSTB[2] I²C-2	PWM2	/	AJ17	DIO
GPIO9	SCLK[3] I²C-3	/	/	AK17	DIO
GPIO10	SDA[3] I²C-3	/	/	AM17	DIO
GPIO11	SRSTB[3] I²C-3	PWM3	/	AM21	DIO
GPIO12	SCLK[4] I²C-4	/	/	AL21	DIO
GPIO13	SDA[4] I²C-4	/	/	AJ20	DIO
GPIO14	SRSTB[4] I²C-4	PWM4	/	AN21	DIO
GPIO15	SCLK[5] I²C-5	/	/	AK20	DIO
GPIO16	SDA[5] I²C-5	/	/	AK16	DIO
GPIO17	SRSTB[5] I²C-5	PWM5	/	AN17	DIO
GPIO18	SCLK[6] I²C-6	/	/	AM20	DIO

GPIO19	SDA[6] I²C-6	/	/	AL18	DIO
GPIO20	SRSTB[6] I²C-6	PWM6	/	AL16	DIO
GPIO21	SCLK[7] I²C-7	/	/	AM16	DIO
GPIO22	SDA[7] I²C-7	/	/	AM18	DIO
GPIO23	SRSTB[7] I²C-7	PWM7	/	AN18	DIO
GPIO24	SCLK[8] I²C-8	/	/	AN16	DIO
GPIO25	SDA[8] I²C-8	/	/	AM15	DIO
GPIO26	SRSTB[8] I²C-8	PWM8	/	AN15	DIO
GPIO27	SCLK[9] I²C-9	/	/	AK15	DIO
GPIO28	SDA[9]	/	/	AJ15	DIO
GPIO29	SRSTB[9] I²C-9	PWM9	/	AN13	DIO
GPIO30	SCLK[10] I²C-10	/	/	AN14	DIO
GPIO31	SDA[10] I²C-10	/	/	AM13	DIO
GPIO32	SRSTB[10] I²C-10	PWM10	/	AM14	DIO
GPIO33	SCLK[11] I²C-11	/	/	AJ13	DIO
GPIO34	SDA [11] I²C-11	/	/	AL14	DIO
GPIO35	SRSTB [11] I²C-11	PWM11	/	AK13	DIO
GPIO36	USOUT[0] UART-0	/	/	AK14	DIO
GPIO37	USIN[0] UART-0	/	/	AN11	DIO
GPIO38	USOUT[1] UART-1	/	/	AM11	DIO
GPIO39	USIN[1] UART-1	/	/	AN12	DIO
GPIO40	USOUT[2] UART-2	/	/	AK11	DIO
GPIO41	USIN[2] UART-2	/	/	AJ11	DIO
GPIO42	USOUT[3] UART-3	/	/	AN10	DIO

GPIO43	USIN[3] UART-3	/	/	AM10	DIO
GPIO44	SPI0_DATA[0]/ MOSI	/	/	AL12	DIO
GPIO45	SPI0_DATA[1]/ MISO	/	/	AM12	DIO
GPIO46	SPI0_DATA[2]	/	/	AM9	DIO
GPIO47	SPI0_DATA[3]	/	/	AL10	DIO
GPIO48	SPI0_CLK	/	/	AN9	DIO
GPIO49	SPI0_CS0B	/	/	AK10	1=boot from SPI, 0= boot from eMMC. Default must pull up to VDDIO2 by 1KΩ Resistor.
GPIO50	SPI0_CS1B	/	/	AK12	DIO
GPIO51	/	/	/	AL8	DIO
GPIO52	/	/	/	AJ9	DIO
GPIO53	/	/	/	AK9	DIO
GPIO54	/	/	/	AN8	DIO
GPIO55	/	/	/	AM8	DIO
GPIO56	AC_GOOD_L	/	/	AK8	DIO
GPIO57	SPI1_CS1B	/	/	A8	DIO
GPIO58	SCLOCK[0] SGPIO-0	/	SCLK[12] I²C-12	B8	DIO
GPIO59	SLOAD[0] SGPIO-0	/	SDA [12] I²C-12	A7	DIO
GPIO60	SDATAOUT[0] SGPIO-0	/	SRSTB [12] I²C-12	D9	DIO
GPIO61	SDATAIN[0] SGPIO-0	PWM12	/	C9	DIO
GPIO62	SCLOCK[1] SGPIO-1	/	SCLK[13] I²C-13	D8	DIO
GPIO63	SLOAD[1] SGPIO-1	/	SDA [13] I²C-13	E10	DIO

GPIO64	SDATAOUT[1] SGPIO-1	/	SRSTB [13] I²C-13	B9	DIO
GPIO65	SDATAIN[1] SGPIO-1	PWM13	/	A9	DIO
GPIO66	SCLOCK[2] SGPIO-2	/	SCLK[14] I²C-14	D12	DIO
GPIO67	SLOAD[2] SGPIO-2	/	SDA [14] I²C-14	E12	DIO
GPIO68	SDATAOUT[2] SGPIO-2	/	SRSTB [14] I²C-14	B10	DIO
GPIO69	SDATAIN[2] SGPIO-2	PWM14	/	D10	DIO
GPIO70	SCLOCK[3] SGPIO-3	/	SCLK[15] I²C-15	B12	DIO
GPIO71	SLOAD[3] SGPIO-3	/	SDA [15] I²C-15	A12	DIO
GPIO72	SDATAOUT[3] SGPIO-3	/	SRSTB [15] I²C-15	D13	DIO
GPIO73	SDATAIN[3] SGPIO-3	PWM15	/	C13	DIO
GPIO74	SPI1_DATA[0]/ MOSI	/	/	A10	DIO
GPIO75	SPI1_DATA[1]/ MISO	/	/	D11	DIO
GPIO76	SPI1_DATA[2]	/	/	B13	DIO
GPIO77	SPI1_DATA[3]	/	/	A13	DIO
GPIO78	SPI1_CLK	/	/	B18	DIO
GPIO79	SPI1_CS0B	/	/	A18	DIO
GPIO80	PWM0	/	SCLOCK[4] SGPIO-4	B11	DIO
GPIO81	PWM1	/	SLOAD[4] SGPIO-4	C11	DIO
GPIO82	PWM2	/	SDATAOUT[4] SGPIO-4	D18	DIO
GPIO83	PWM3	/	SDATAIN[4] SGPIO-4	E18	DIO
GPIO84	PWM4	/	SCLOCK[5] SGPIO-5	A11	DIO

GPIO85	PWM5	/	SLOAD[5] SGPIO-5	B19	DIO
GPIO86	PWM6	/	SDATAOUT[5] SGPIO-5	A19	DIO
GPIO87	PWM7	/	SDATAIN[5] SGPIO-5	C19	DIO
GPIO88	PWM8	/	SCLOCK[6] SGPIO-6	E14	DIO
GPIO89	PWM9	/	SLOAD[6] SGPIO-6	B14	DIO
GPIO90	PWM10	/	SDATAOUT[6] SGPIO-6	D14	DIO
GPIO91	PWM11	/	SDATAIN[6] SGPIO-6	D19	DIO
GPIO92	PWM12	/	SCLOCK[7] SGPIO-7	A20	DIO
GPIO93	PWM13	/	SLOAD[7] SGPIO-7	D15	DIO
GPIO94	PWM14	/	SDATAOUT[7] SGPIO-7	B20	DIO
GPIO95	PWM15	/	SDATAIN[7] SGPIO-7	D20	DIO
GPIO96	PWM16	/	UART0_RTS	A14	DIO
GPIO97	PWM17	/	UART0_CTS	E20	DIO
GPIO98	PWM18	/	UART1_RTS	C15	DIO
GPIO99	PWM19	/	UART1_CTS	B15	DIO
GPIO100	PWM20	/	UART2_RTS	A15	DIO
GPIO101	PWM21	/	UART2_CTS	A21	DIO
GPIO102	PWM22	/	UART3_RTS	E17	DIO
GPIO103	PWM23	/	UART3_CTS	B21	DIO
GPIO104	PWM24	/	/	C21	DIO
GPIO105	PWM25	/	/	D21	DIO
GPIO106	PWM26	/	/	A22	DIO
GPIO107	PWM27	/	/	D17	DIO
GPIO108	PWM28	/	/	B22	DIO
GPIO109	PWM29	/	/	B17	DIO
GPIO110	PWM30	/	/	D22	DIO
GPIO111	PWM31	/	/	A17	DIO
GPIO112	/	/	/	E22	DIO

GPIO113	/	/	/	A23	DIO
GPIO114	/	/	/	D23	DIO
GPIO115	/	/	/	B23	1=SATA,0= UART. Default must pull down to Ground by 1KΩ Resistor.
GPIO116	/	/	/	C23	1=Enable eFuse，0=Disable eFuse. Default is pull up to VDDIO3 by 1KΩ Resistor.
GPIO117	FORCE_ROM	/	/	E23	0=Force ROM, 1= Normal Mode. Default must pull up to VDDIO3 by 1KΩ Resistor.

3.2.5. JTAG Interface (RFU)

The JTAG interface is designed for boundary scan purpose. The JTAG function is not supported yet .The related Pins is reserved for future use.

Table 3.5 JTAG Interface Signals(RFU)

Signal Name	Description	Signal Number	Type
JTAG_TDI	Test Access Data Input,1.8V CMOS Digital Input Internal Pull-up	AL30	DI
JTAG_TDO	Test Access Data Output,1.8V CMOS open drain Output,Tri-stated	AL29	OD
JTAG_TCK	Test Access Port Clock,1.8V CMOS Digital Input	AM30	DI
JTAG_TMS	Test Access Mode Select,1.8V CMOS Digital Input Internal Pull-up	AL28	DI
JTAG_TRSTN	Active low Test Access Reset,1.8V CMOS Digital Input Internal Pull-up	AL31	DI

3.2.6. eMMC Interface

Table 3.6 eMMC Interface Signals

Signal Name	Description	Signal Number	Type
E0_HCMD	**eMMC Command/Response，1.8V Input/Output** command: a command is a token that starts an operation. A command is sent from the host to a device . A command is transferred serially on the CMD line. response: a response is a token that is sent from the device to the host as an answer to a previously received command. A response is transferred serially on the CMD line.	AN26	DIO
E0_HCLK	**eMMC Clock，1.8V Output**	AL24	DO
E0_HDATA0	**eMMC Data，1.8V Input/Output** data can be transferred from the device to the host or vice versa. Data is transferred via the data lines. The number of data lines used for the data transfer can be 4(DAT0-DAT3) or 8(DAT0-DAT7).	AJ25	DIO
E0_HDATA1		AN25	DIO
E0_HDATA2		AK25	DIO
E0_HDATA3		AM25	DIO
E0_HDATA4		AK24	DIO
E0_HDATA5		AL26	DIO
E0_HDATA6		AM26	DIO
E0_HDATA7		AM24	DIO

3.2.7. Power Supply

Table 3.7 Power Interface

Pin Name	Description	Pin Number	Type
AVDL0	PHY0/1/2/3/4/5: 0.9V analog core power supply.	K6,L1,L7,M6,M8,M26,M32,M33,N1,N7,N9,N25,P6,P8,P10,P24,P26,R1,R7,R9,R11,R23,R25,T6,T8,T10,T24,T26,U7,U9,U11,U22,U23,U25,U32,U33,V6,V8,V10,V24,V26,W1,W7,W9,W11,W22,W23,W25,Y6,Y8,Y10,Y12,Y24,AA1,AA7,AA9,AA11,AA23,AA26,AB6,AB8,AB10,AB12,AB22,AB25,AB32,AB33,AC1,AC7,AC9,AC11,AC24,AC26,AD6,AD8,AD10,AD23,AD25,AE7,AE9,AE24,AE26,AF6,AF8,AF25,AG1,AG7,AG24,AG26,AG32,AG33,AH6,AH25,AJ1,AJ26,AK27	PI
AVDL1	PHY6/7/8: 0.9V	A3,A26,A28,A30,A32,B6,B27,B29,B31,C1,C7,C25,D6,	PI

	analog core power supply.	D26,E1,E7,E25,F6,F8,F26,G1,G7,G25,G27,G32,G33, H6,H8,H10,H24,J7,J9,J11,J25,J26,K8,K10,K12,K24, L9,L11,L13,L23,L25,M10,M24,N11,N22,N23,R22	
AVDH0	PHY0/1/2/3/4/5: 1.8V analog IO power supply.	P12,R13,T12,T22,U13,U21,V12,V22,W13,W21,Y22, AA21	PI
AVDH1	PHY6/7/8: 1.8V analog IO power supply.	M12,M22,N13,N21,P22,R21	PI
VDDK	Digital core power supply for logical cell, 0.9V.	N15,N17,N19,P16,P18,R15,R17,R19,T16,T18,U15, U17,U19,V16,V18,W15,W17,W19,Y16,Y18	PI
VDDIO18	IO power switch for the level shifters and pre-drivers, 1.8V.	A24,B24,C24,D24,E24,F24,G12,G16,G20,G24,H13,H15,H17,H19,H21,H23,J14,J16,J18,J20,J22,K15,K17,K19, K21,L16,L18,L20,AB15,AB17,AB19,AC14,AC16, AC18,AC20,AD13,AD15,AD17,AD19,AD21,AE12, AE14,AE16,AE18,AE20	PI
VDDIO1	IO power supply 1.8V for the eMMC/JTAG/SEL3VU/SEL3VD and reset signal.	AE22,AF21,AF23,AG21,AG22,AH22,AH23,AJ23, AJ24,AK23,AL23,AM23,AN23	PI
VDDIO2	IO power supply 1.8/3.3V for GPIO0~56. 1.8/3.3V voltage is selected by SEL3VU.	AF12,AF14,AF16,AF18,AF20,AG11,AG13,AG15, AG17,AG19,AH10,AH12,AH14,AH16,AH18,AH19, AH20,AJ19,AK19,AL19,AM19,AN19	PI
VDDIO3	IO power supply 1.8/3.3V for GPIO57~117. 1.8/3.3V voltage is selected by SEL3VD.	A16,B16,C16,C18,D16,F9,F11,F13,F15,F17,F19,F21, F23,G10,G14,G18,G22	PI
VCC18_CPOR	Power Supply 1.8V for the chip's Power On Reset POR, Voltage detection and Junction temperature detection.	AA13	PI
VDDA_XTAL	XTAL power supply	AC23	PI

	1.8V.		
VDDA_PLL	PLL power supply 1.8V. Default is no connection.	AB20	PI
VDDQ_ROM	eFuse 1.8V power supply.	AC21	PI
VSS	Analog and Digital ground.	A2,A6,A25,A27,A29,A31,B3,B4,B5,B7,B25,B26,B28,B30,B32,B33,C2,C3,C6,C8,C10,C12,C14,C17,C20,C22,C26,C29,C30,D3,D4,D5,D7,D25,D27,D30,D31,E2,E3,E6,E9,E11,E13,E15,E16,E19,E21,E26,E29,E30,F3,F4,F5,F7,F10,F12,F14,F16,F18,F20,F22,F25,F27,F30,F31,G2,G3,G6,G8,G9,G11,G13,G15,G17,G19,G21,G23,G26,G28,G29,G30,G31,H3,H4,H5,H7,H9,H11,H12,H14,H16,H18,H20,H22,H25,H26,H29,H30,J1,J2,J3,J6,J8,J10,J12,J13,J15,J17,J19,J21,J23,J24,J27,J30,J31,K3,K4,K5,K7,K9,K11,K13,K14,K16,K18,K20,K22,K23,K25,K26,K29,K30,L2,L3,L6,L8,L10,L12,L14,L15,L17,L19,L21,L22,L24,L26,L27,L30,L31,M3,M4,M5,M7,M9,M11,M23,M25,M27,M28,M29,M30,M31,N2,N3,N6,N8,N10,N12,N16,N18,N24,N26,N29,N30,P3,P4,P5,P7,P9,P11,P15,P17,P19,P23,P25,P27,P30,P31,R2,R3,R6,R8,R10,R12,R16,R18,R24,R26,R29,R30,T3,T4,T5,T7,T9,T11,T15,T17,T19,T23,T25,T27,T30,T31,U1,U2,U3,U6,U8,U10,U12,U16,U18,U24,U26,U27,U28,U29,U30,U31,V3,V4,V5,V7,V9,V11,V15,V17,V19,V23,V25,V29,V30,W2,W3,W6,W8,W10,W12,W16,W18,W24,W26,W27,W30,W31,Y3,Y4,Y5,Y7,Y9,Y11,Y13,Y15,Y17,Y19,Y23,Y25,Y26,Y29,Y30,AA2,AA3,AA6,AA8,AA10,AA12,AA22,AA24,AA25,AA27,AA30,AA31,AB3,AB4,AB5,AB7,AB9,AB11,AB16,AB18,AB21,AB23,AB24,AB26,AB27,AB28,AB29,AB30,AB31,AC2,AC3,AC6,AC8,AC10,AC15,AC17,AC19,AC22,AC25,AC29,AC30,AD3,AD4,AD5,AD7,AD9,AD14,AD16,AD18,AD20,AD22,AD24,AD26,AD27,AD30,AD31,AE1,AE2,AE3,AE6,AE8,AE13,AE15,AE17,AE19,AE21,AE23,AE25,AE27,AE28,AE29,AE30,AE31,AE32,AE33,AF3,AF4,AF5,AF7,AF11,AF13,AF15,AF17,AF19,AF22,AF24,AF26,AF29,AF30,AG2,	Ground

		AG3,AG6,AG10,AG12,AG14,AG16,AG18,AG20, AG23,AG25,AG27,AG28,AG29,AG30,AG31,AH3, AH4,AH5,AH9,AH11,AH13,AH15,AH17,AH21,AH24, AH26,AH29,AH30,AJ2,AJ3,AJ10,AJ12,AJ14,AJ16, AJ18,AJ21,AJ27,AJ30,AJ31,AK3,AK4,AK5,AK28, AK29,AK32,AK33,AL1,AL2,AL3,AL9,AL11,AL13, AL15,AL17,AL20,AL22,AL25,AL27,AL32,AL33, AM3,AM4,AM5,AM28,AM31,AN2,AN3,AN32	

Caution：

If certain PIN's pull up/down is needed,

1. For eMMC, JTAG or PORSTN signals pull up, they must be connected to VDDIO1 with resistor;

2. For SEL3VU and SEL3VD they must be connected to the standby power (the pre-start power source) or VDDIO1 with resistor;

3. For eMMC, JTAG, SEL3VU, SEL3VD and GPIO0~117 signal, the pull up/pull down must be done before PORSTN is released;

4. It is not acceptable if GPIO0~56 pulling up to 3.3V is prior to 1.8V power rail ramps;

5. Specifically, if the ROM booting start from SFLASH, SPI0_CS0B(GPIO49) must be pulled up before PORSTN is released.

3.2.8. Miscellaneous Pins

Table 3.8 Miscellaneous Interface

Pin Name	Description	Pin Number
NC	Pin is floating and is not connected internally to any active circuitry nor has any electrical continuity to any other pin.	A1,A33,C33,E33,H33,K33,N33,R33,V33,Y33, AB13,AB14,AC12,AC13,AC33,AD11,AD12, AE10,AE11,AF9,AF10,AF33,AG8,AG9,AH7, AH8,AH33,AJ6,AJ7,AJ8,AK6,AK7,AL6,AL7, AM6,AM7,AN1,AN6,AN7,AN29,AN33
DNC	Device pin to which there may or may not be an internal connection, but to which no external connection are allowed.	AK30,AK31,E8,AF32,AF31,AJ4,AJ5,AL30,AL29,AM30,AL28,AL31

CHAPTER 4 ELECTRICAL CHARACTERISTICS

4.1. Absolute Maximum Rating

Table 4.1 Absolute Maximum Rating

Parameter	Symbol	Min	Typical	Max/高温	Units
Absolute IO Power Supply 3.3V[1]	VDDIO2/3	-0.3	/	3.93	V
Absolute IO Power Supply 1.8V[1]	VDDIO1/2/3	-0.3	/	2.28	V
Absolute Core Power Supply 0.9V[1]	VDDK	-0.2	/	1.29	V
Absolute Analog Power Supply 1.8V[1]	AVDH0/1	-0.3	/	2.28	V
Absolute Analog Power Supply 0.9V[1]	AVDL0/1	-0.2	/	1.29	V
Absolute Storage Temperature[1]	$T_{STORAGE}$	-40	/	125	ºC
Absolute Junction Temperature[1]	Tj	/	/	125	ºC
MSL Level[1]		4			
HBM ESD[1]		≥2KV			
CDM ESD[1]		≥250V			

CAUTION: Exposure to conditions at or beyond the maximum rating may damage the device . Operation beyond the recommended operating conditions (Table 4.2) is neither recommended nor guaranteed.

Note[1]: According to LAB measured test result.

4.2. Recommended Operating Condition

Table 4.2 Operating Voltage and Temperature

Parameter	Symbol	Min	Typical	Max	Units
Digital 1.8V power supply[3]	VDDIO1/2/3/18	1.71	1.8	1.89	V
Digital 3.3V power supply[3]	VDDIO2/3	3.135	3.3	3.465	V
Digital core power supply[3]	VDDK	0.855	0.9	0.945	V

Analog 1.8V power supply[3]	AVDH0/1	1.71	1.8	1.89	V
Analog 0.9V power supply[3]	AVDL0/1	0.855	0.9	0.945	V
Ripple of AVDL0/1[2]	The ripple and noise of the power DC	0	/	27	mV
Ripple of AVDH0/1[2]		0	/	54	mV
Ripple of VDDK[2]		0	/	27	mV
Ripple of VDDIO1/2/3[2]		0	/	54	mV
Ambient Operating Temperature[1]	Ta	0	25	70	ºC
Junction Operating Temperature[1]	Tj	0	/	105	ºC

CAUTION: Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

Note[1]: According to LAB measured test result.

Note[2]: According to Design Specification.

Note[3]: According to FT measured test result.

4.3. I/O DC Characteristics

The 3.3V IO cell support 3.3V LVTTL level. The 3.3V IO DC characteristic is shown as below,

Table 4.3 IO DC Character Operating at 3.3V

Parameter	Symbol	Min	Typical	Max	Units
Input leakage current[3]	IiL (Vin=0V)	/	±1.0（FT）	±10	μA

Input leakage current[3]	IiH (Vin=VDDIO)	/	±1.0（FT）	±10	μA
Input pull-up resistance[2]	Rpu (Vin= 0V)	20	40	100	KΩ
Input pull-down resistance[2]	Rpd (Vin= VDDIO)	20	40	100	KΩ
Input low voltage[1]	ViL	/	/	0.3*VDDIO	V
Input high voltage[1]	ViH	0.7*VDDIO	/	/	V
Output low voltage[3]	V_{OL} (IoL=4.0mA~16mA)	/	/	0.4	V
Output high voltage[3]	V_{OH} (IoH=4.0mA~16mA)	2.4	/	/	V

The 1.8V IO cell support 1.8V CMOS level. The 1.8V IO DC characteristic is shown as below,

Table 4.4 IO DC Character Operating at 1.8V

Parameter	Symbol	Min	Typical	Max	Units
Input leakage current[3]	IiL (Vin=0V)	/	±1.0	±10	μA
Input leakage current[3]	IiH (Vin=VDDIO)	/	±1.0	±10	μA
Input pull-up resistance[2]	Rpu (Vin= 0V)	10	22	55	KΩ
Input pull-down resistance[2]	Rpd (Vin= VDDIO)	10	22	55	KΩ
Input low voltage[1]	ViL	/	/	0.3*VDDIO	V
Input high voltage[1]	ViH	0.7*VDDIO	/	/	V
Output low voltage[3]	V_{OL} (IoL=3.0mA~12mA)	/	/	0.4	V
Output high voltage[3]	V_{OH} (IoH=3.0mA~12mA)	1.35	/	/	V

4.4. Power Supply DC Characteristics

Table 4.5&4.6 defines the Power Supply for HL7721 according to measured results. The Power

Supply Test Condition is as follows,

Minimum: The chip is on idle mode.

Typical: The chip is on full load/full speed IO running @Ta=25℃.

Maximum: The chip is on full load/full speed IO running @Ta=70℃.

Table 4.5 HL7721 Power Supply Condition for VDDIO2/VDDIO3=1.8V[1]

Parameter	Symbol	Min	Typical	Max	Units
Analog 1.8V power supply	AVDH0+AVDH1	340	360	380	mA
Analog 0.9V power supply	AVDL0+AVDL1	1250	3600	3990	mA
Digital 0.9V core power supply	VDDK	2580	3320	4950	mA

Table 4.6 HL7721 Power Supply Condition for VDDIO2/VDDIO3=3.3V[1]

Parameter	Symbol	Min	Typical	Max	Units
Analog 1.8V power supply	AVDH0+AVDH1	340	360	380	mA
Analog 0.9V power supply	AVDL0+AVDL1	1230	3730	4260	mA
Digital 0.9V core power supply	VDDK	2590	3380	5000	mA

Note[1]: According to LAB measured test result.

Caution：

If all GPIO PIN's is working in output mode, it need to increase power supply for VDDIO2/3. Since GPIO's IOL/IOH is between 4mA to 12mA when operating at 1.8V, Table 4.7 defines the Power Supply for VDDIO2/3 in maximum.

Table 4.7 Power Supply Condition for VDDIO2/VDDIO3=1.8V[2]

Parameter	Symbol	One GPIO Condition	GPIO Number	Power Supply	Units
GPIO0~GPIO56 power supply	VDDIO2	12	57	684	mA
GPIO57~GPIO117 power supply	VDDIO3	12	61	732	mA

Note[2]: According to Design Specification.

GPIO's IOL/IOH is between 4mA to 16mA when operating at 3.3V. The Table 4.8 defines the Power Supply for VDDIO2/3 in maximum.

Table 4.8 Power Supply Condition for VDDIO2/VDDIO3=3.3V[2]

Parameter	Symbol	One GPIO Condition	GPIO Number	Power Condition	Units
Digital 3.3V power supply	VDDIO2	16	57	912	mA
Digital 3.3V power supply	VDDIO3	16	61	976	mA

Note[2]: According to Design Specification.

4.5. System Clock Specification

4.5.1 System Clock Description

Table 4.9 System Clock Description[1]

Clock Domain	Frequency	Source
XTALI, XTALO	25MHz	25MHz Crystal/Oscillator
PHY0_CKREFP, PHY0_CKREFN	100MHz	PLL take the external clock to generate high speed clock for data transmitting and receiving. The differential 100MHz clock is fed to PHY0, effective for PHY0[0:3]~PHY8[0:3]

Note[1]: According to Lab measured result.

4.5.2 System Clock Input Frequency Specification

Table 4.10 Crystal/Oscillator AC Specification[1]

Symbol	Parameter	Min	Typical	Max	Units
fxtal	Frequency	/	25	/	MHz
Δfxtal	Long Term Stability	-50	/	50	ppm

Note[1]: According to Lab measured result.

4.6. Thermal Data

Table 4.10 provides the thermal data for the HL7721. The simulation was performed based on JEDEC specification.

Table 4.11 Package Thermal Data[3]

Parameter	Parameter	Data
θ_{JA}	Thermal Resistance: Junction To Ambient	8.73℃/W @Ta=25℃ 7.99℃/W @Ta=70℃
θ_{JB}	Thermal Resistance: Junction To PCB board	1.82℃/W
θ_{JC}	Thermal Resistance: Junction To Top Center of the LID	0.57℃/W

Note[3]: The simulated data is only for reference, and it is to be used carefully and to be verified by the experiment.

4.7. Power Up/Power Down Condition

Table 4.11 provides the rising edge rate and falling edge rate for VCC 0.9/1.8/3.3V.

Table 4.12 Power Up/Down Condition[1]

Symbol	Parameter	MIN	MAX	Unit
Tvcc	Rising Edge Rate	2900	20000	us/V
	Falling Edge Rate	/	20000	

Note[1]: According to Lab measured result.

CHAPTER 5 POWER SEQUENCE AND RESET TIMING

The power-on sequence is defined in Figure 5.1~5.3. Designers should follow the rules for external power designs as 0.9V->1.8V->3.3V-> PORSTN. Three cases of power sequence is shown depending on different GPIO voltages selection.

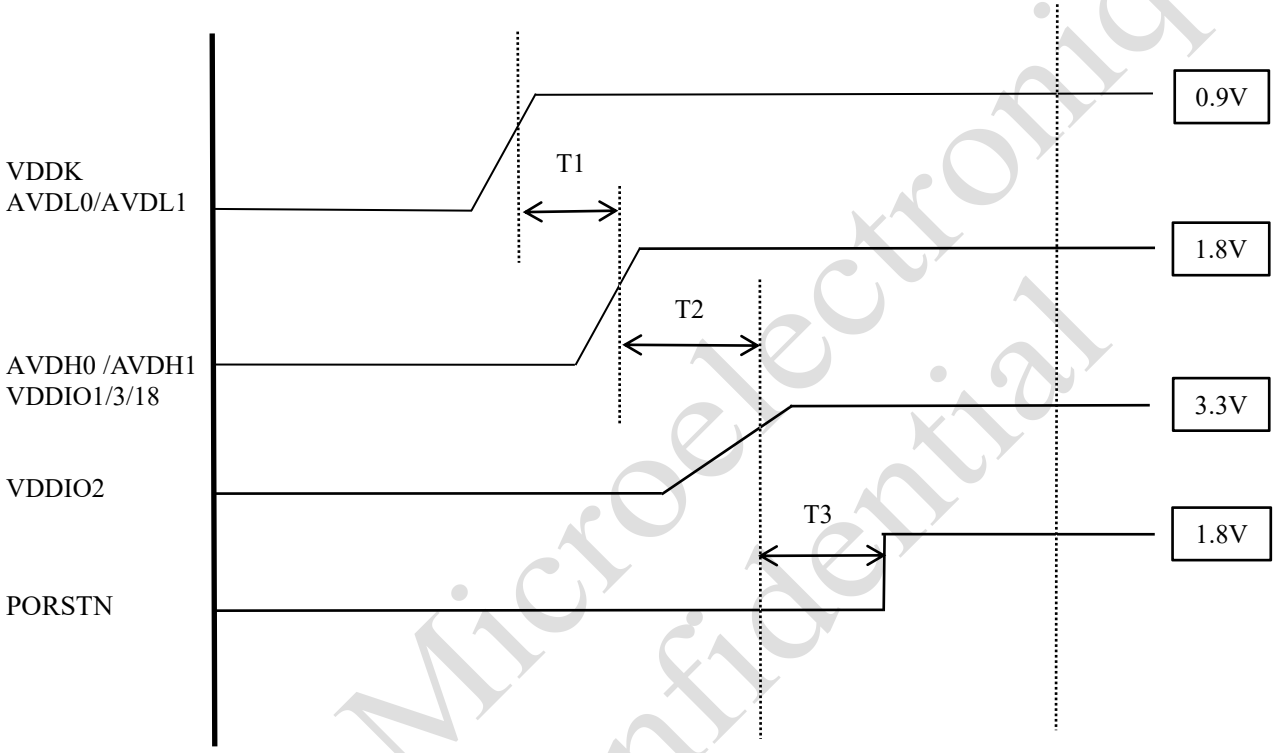


Figure 5.1 Case1: GPIO0~56 3.3V, GPIO57~117 1.8V

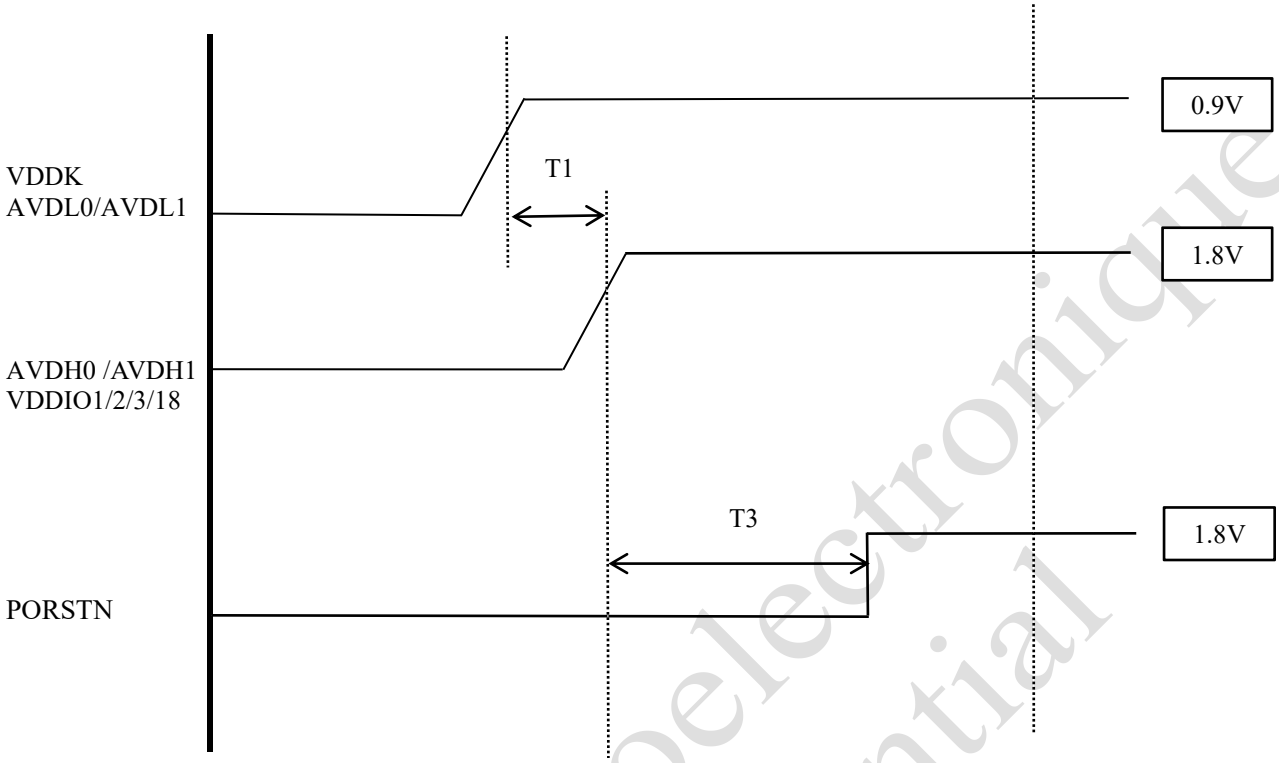


Figure 5.2 Case2: GPIO0~117 1.8V

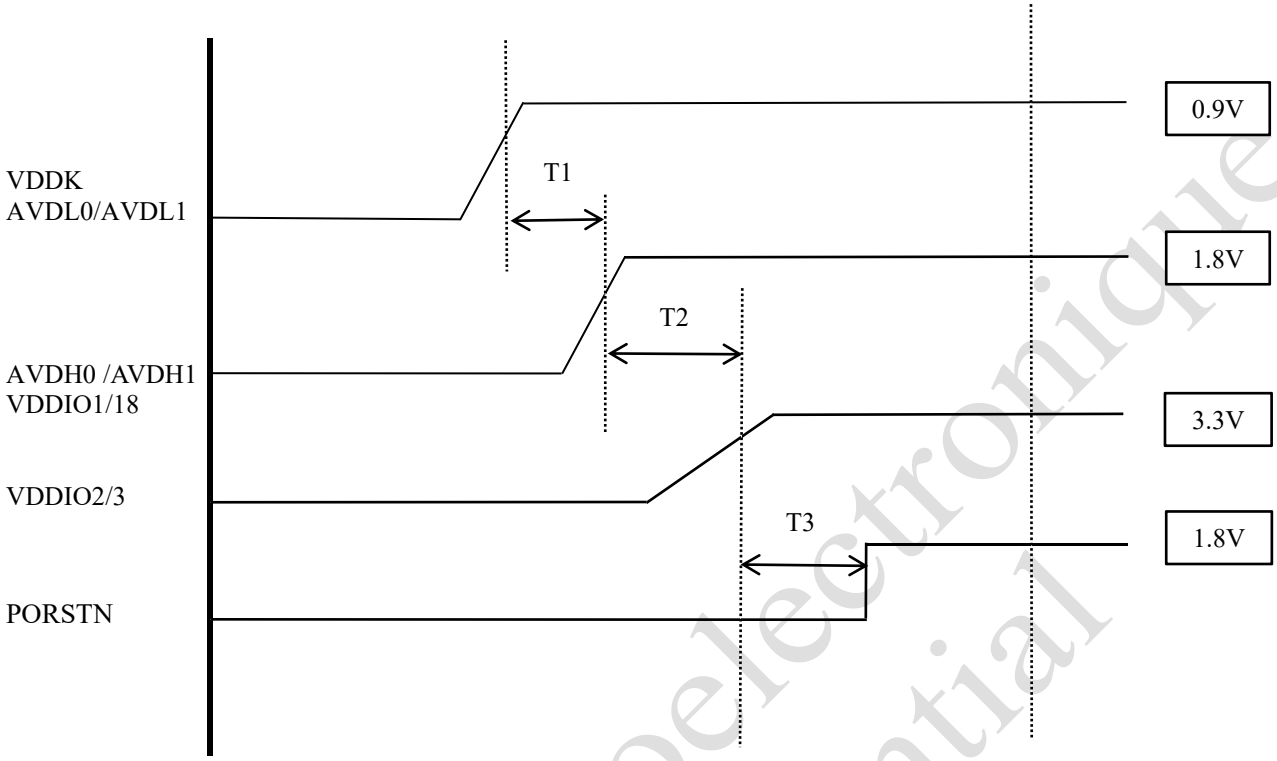


Figure 5.3 Case3: GPIO0~117 3.3V

Table 5.1 Power ON Timing Requirements[1]

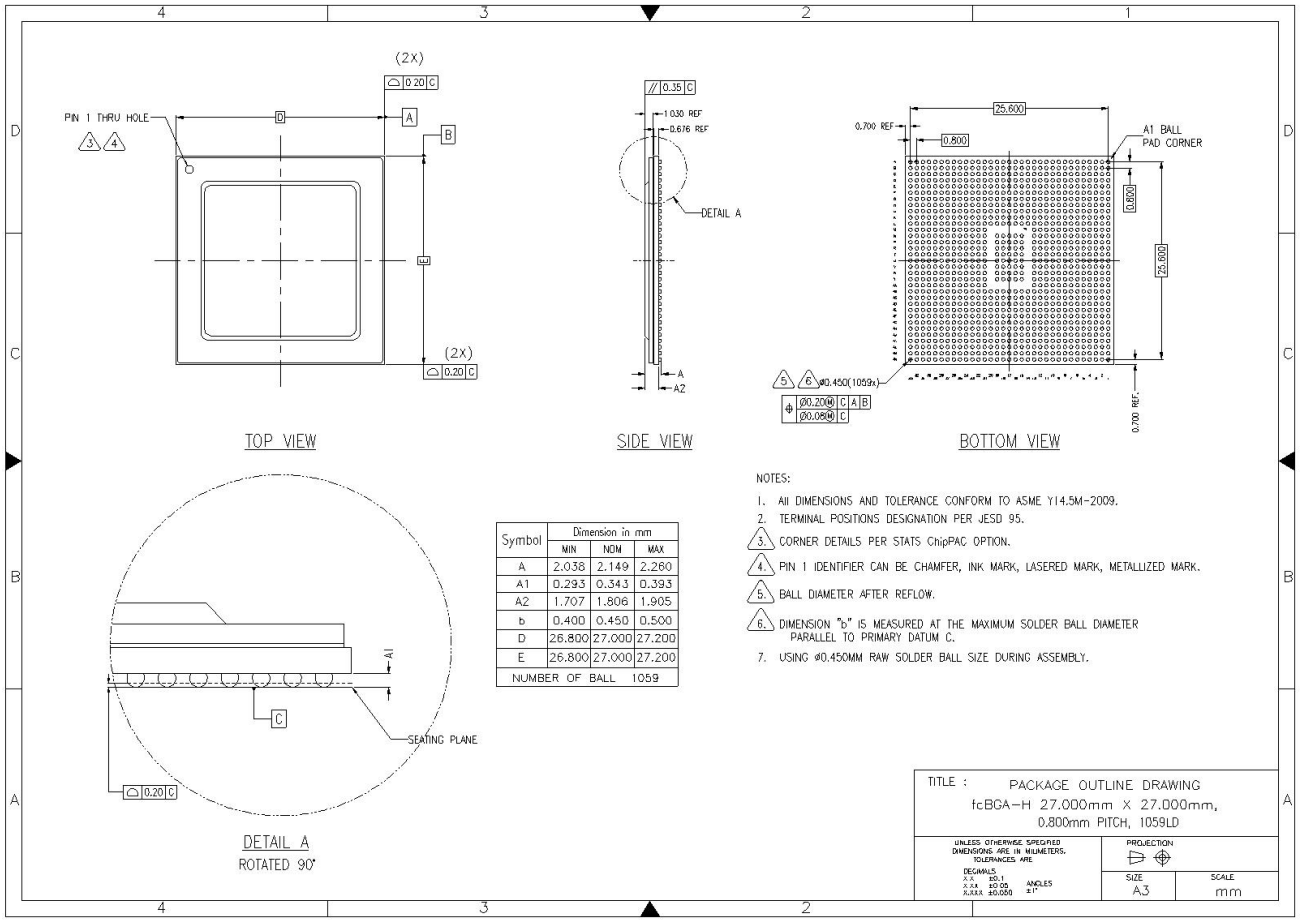
Time	Min	Typical	Max
T1	3ms	/	20ms
T2	2ms	/	20ms
T3	50ms	/	1200ms

Note[1]: According to Lab measured result.

CHAPTER 6 PACKAGE INFORMATION

6.1 Mechanical Drawing

Figure 6.1 shows the mechanical drawing for the HL7721.



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	2.038	2.149	2.260
A1	0.293	0.343	0.393
A2	1.707	1.806	1.905
b	0.400	0.450	0.500
D	26.800	27.000	27.200
E	26.800	27.000	27.200
NUMBER OF BALL 1059			

Figure 6.1 Package Outline Drawing of FCBGA1059 27*27mm